Attorney Docket No. MSC-22953-3

IN THE SPECIFICATION

Please enter the following replacement paragraph(s) from page 3, which starts at line 21 and ends at line 27:

In general, in another aspect, the invention features an SEU-resistant circuit comprising a logic gate having an input and an output and a feedback path from the output of the logic gate to the input of the logic gate. The feedback path comprises two or more delay elements. The logic gate and the two or more delay elements are configured to absorb a standard glitch at the input to the gate before it propagates through the feedback path to the input of the logic gate. The delay is spread among the logic gate and the two or more delay elements.

Please enter the following replacement paragraph(s) from page 3, which starts at line 28 and ends at line 30:

Implementations of the invention may include one or more of the following. The delay may be substantially evenly spread among the logic gate and the two or more delay elements. The delay elements may comprise balanced logic gates. The feedback path may

Please enter the following replacement paragraph(s) from page 4:

The feedback path may further comprise a driver logic gate. The delay elements may comprise inverters. The number of delay elements may be even.

Please enter the following replacement paragraph(s) from page 6, which starts at line 23 and ends at line 27:

In general, in another aspect, the invention features a method for reducing the vulnerability of a latch to single event upsets. The latch comprises a logic gate having an input and an output and a feedback path from the output to the input of the logic gate. The method comprises inserting a delay into the feedback path, and providing a delay in the logic gate.

Please enter the following replacement paragraph(s) from page 7, which starts at line 1 and ends at line 7:

parasitic capacitance of the node. Adjusting may comprise increasing the length of the channel of the first FET. Increasing may comprise making the channel non-linear. Making may comprise inserting a jog into the channel. The jog may be a right angle. The output of the logic gate may be coupled to a threshold device having an input, an output and a threshold. The output may have a first value when the input is less than the threshold and a second value when the input is greater than the threshold.

Please enter the following replacement paragraph(s) from page 9, which starts at line 19 and ends at line 27:

The figures show the FET channel dimensions, length (L) and width (W), relative to lambda, represented by "1" or "8." Lambda is one half the minimum gate length, which means that the minimum gate length will be ~~2= lambda~~ 2*lambda. For some scalable design rules, lambda may deviate slightly. The examples described herein are for an HP 0.5: (0.5 micron) N-well process with lambda=0.3 micron, and nominal load fan out of 10, giving a worst case propagation delay of 1 ns (nanosecond). It will be understood by persons of ordinary skill in the art that a conversion into any particular process may require scaling in order to achieve the required timing properties. In many cases, such a conversion requires little or no adjustment to the lambda-relative dimensions.

Please enter the following replacement paragraph(s) from page 29, which starts at line 7 and ends at line 21:

A delay circuit includes a first network having an input and an output node, a second network having an input and an output, the input of the second network being coupled to the output node of the first network. The first network and the second network are configured such that: a glitch at the input to the first network having a length of approximately one-half of a standard glitch time or less does not cause the voltage at the output of the second network to cross a threshold, a glitch at the input to the first network having a length of between approximately one-half and two standard glitch times causes the voltage at the output of the second network to cross the threshold for less than the length of the glitch, and a glitch at the input to the first network having a length of greater than approximately two standard glitch times causes the voltage at the output of the second network to cross the threshold for approximately the time of the glitch. [The] A method reduces the vulnerability of a latch to single event upsets. The latch includes a logic gate having an input and an output and a feedback path from the output to the input of the logic gate. The method includes inserting a delay into the feedback path and providing a delay in the logic gate.